

Variable Dielectric Delay Lines in Liquid Crystals for Phased Array Feeds

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Outline

PHAROS

- General description
- Vivaldi array, beam former
- Noise temperature test setup and results

Liquid crystal delay line

- General description
- First generation
- Second generation
- Third generation

Conclude and future plan

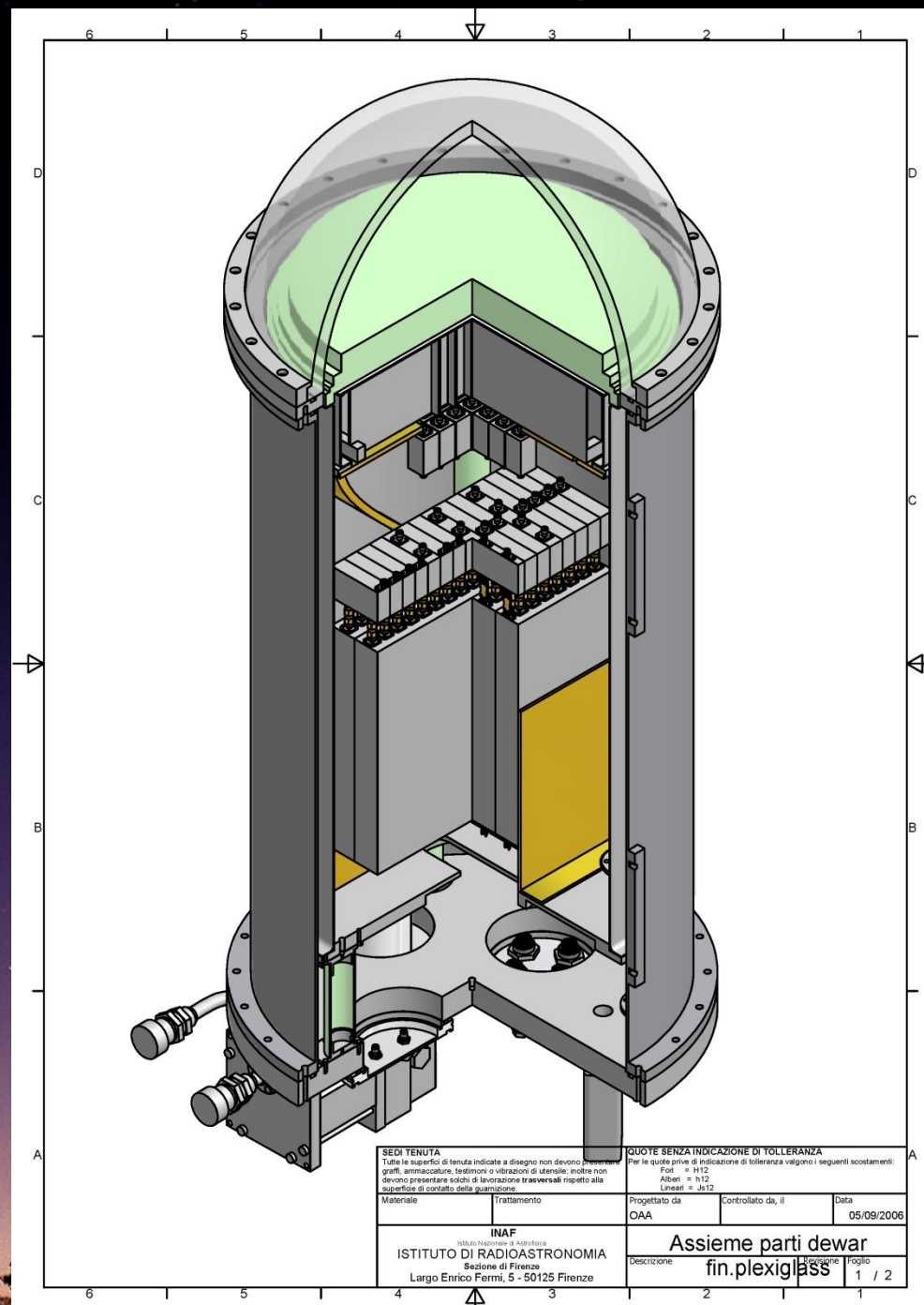


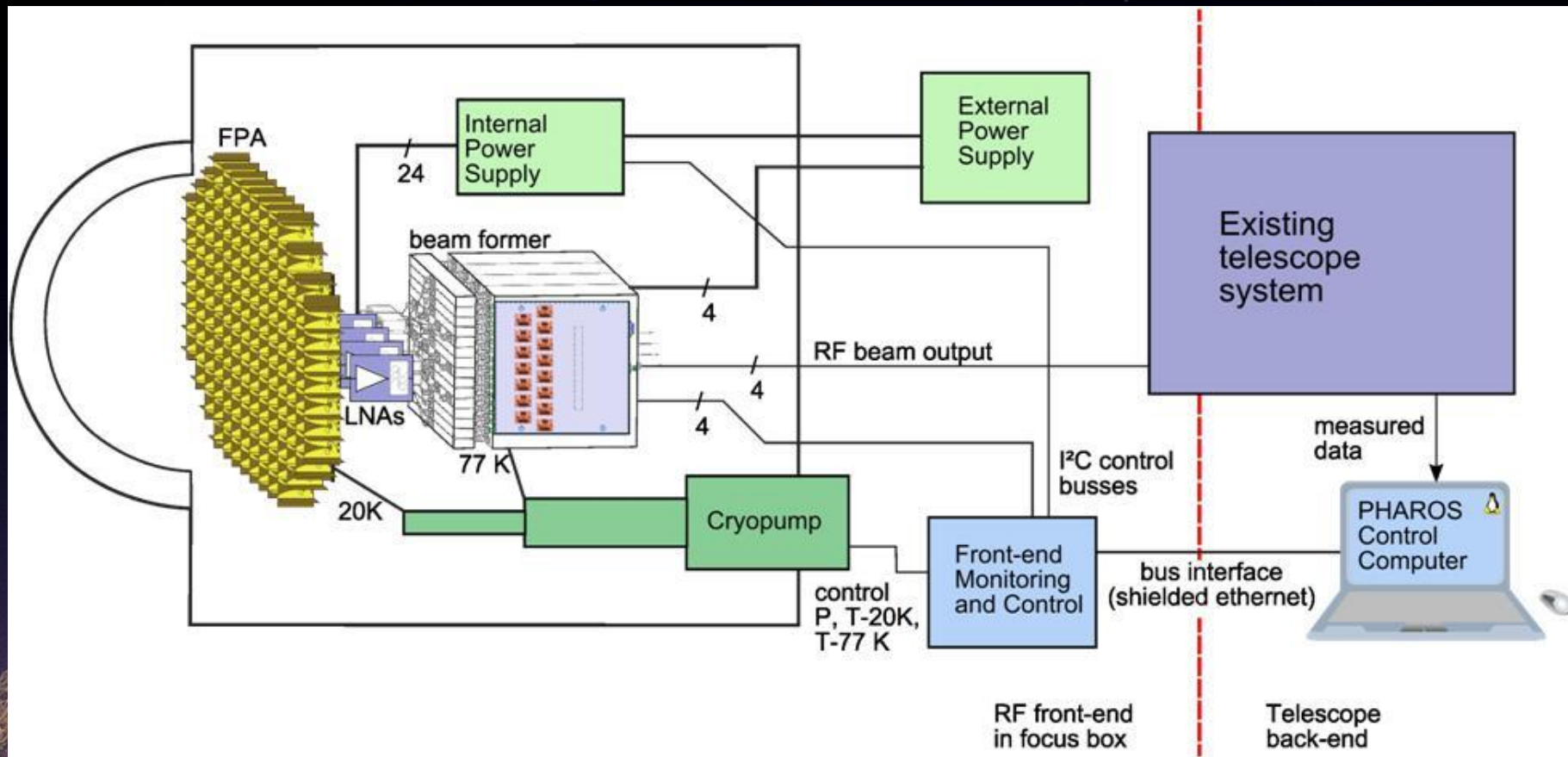
PHased Arrays for Reflector Observing Systems (PHAROS)

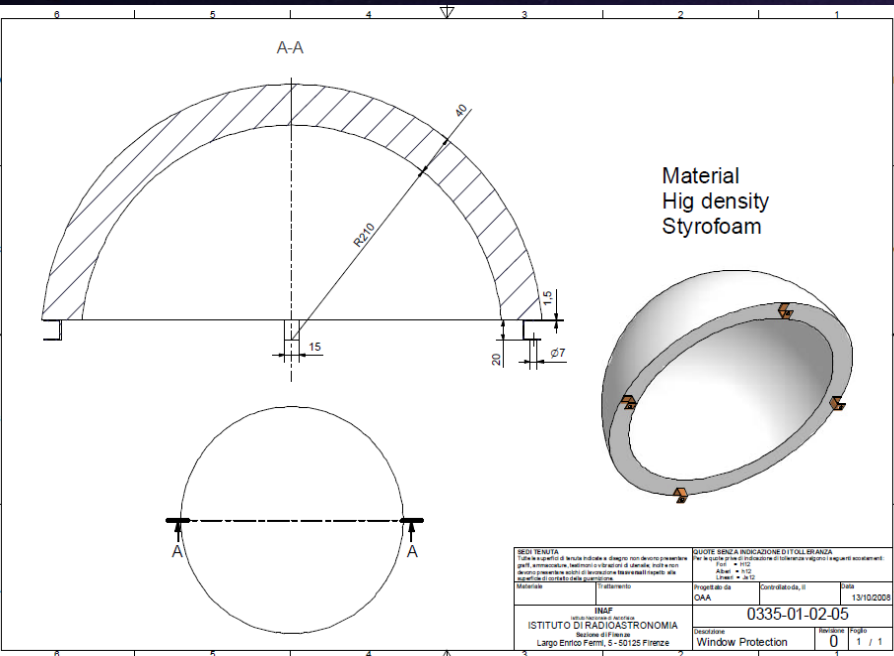
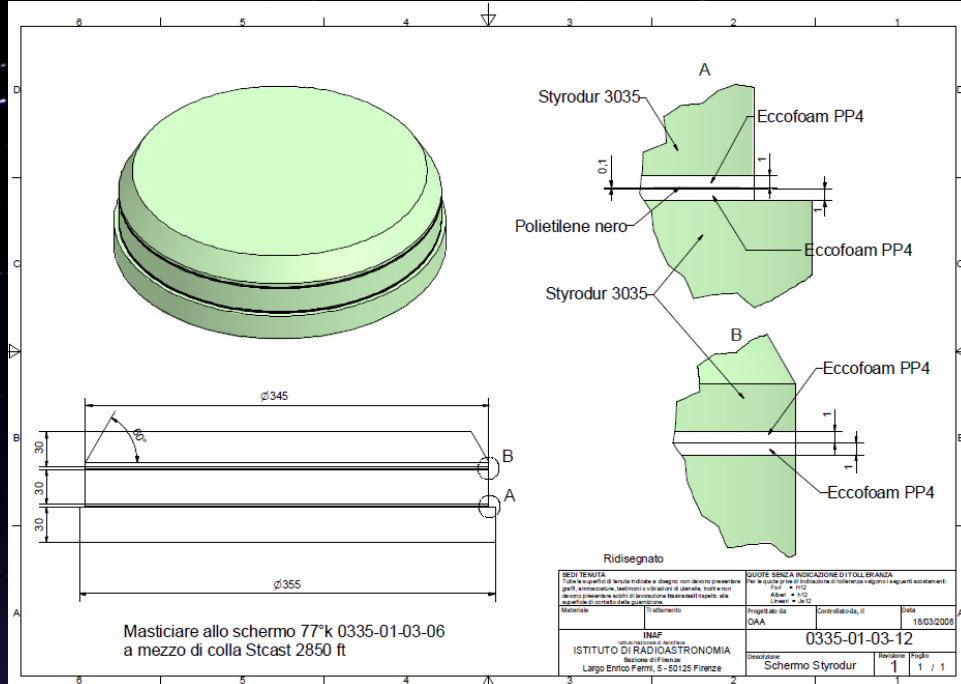
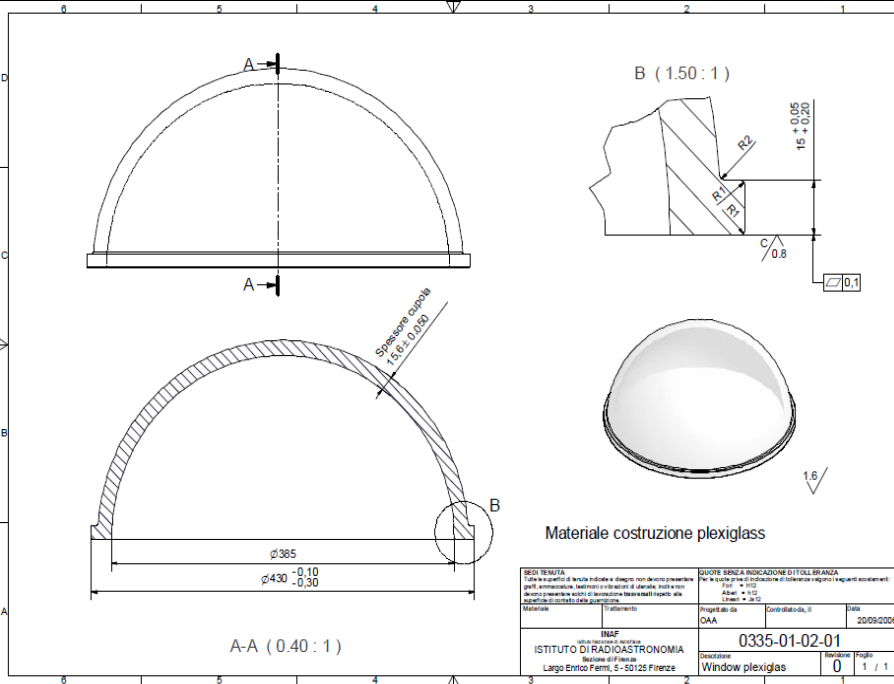
- The key objective of PHAROS is to continue, and bring to fruition, some of the strategic research, begun in the FP5 RTD programme FARADAY (HPRI-CT-2001-50031)
- The partners in PHAROS are Jodrell Bank Observatory (JBO), University of Birmingham, Istituto di Radioastronomia (INAF), Microwave Engineering Centre for Space Applications (MECSA), Nicolaus Copernicus University (TCfA), Commonwealth Science and Industrial Research Organization (CSIRO) and Netherlands Foundation for Research in Astronomy (ASTRON)



What PHAROS looks like

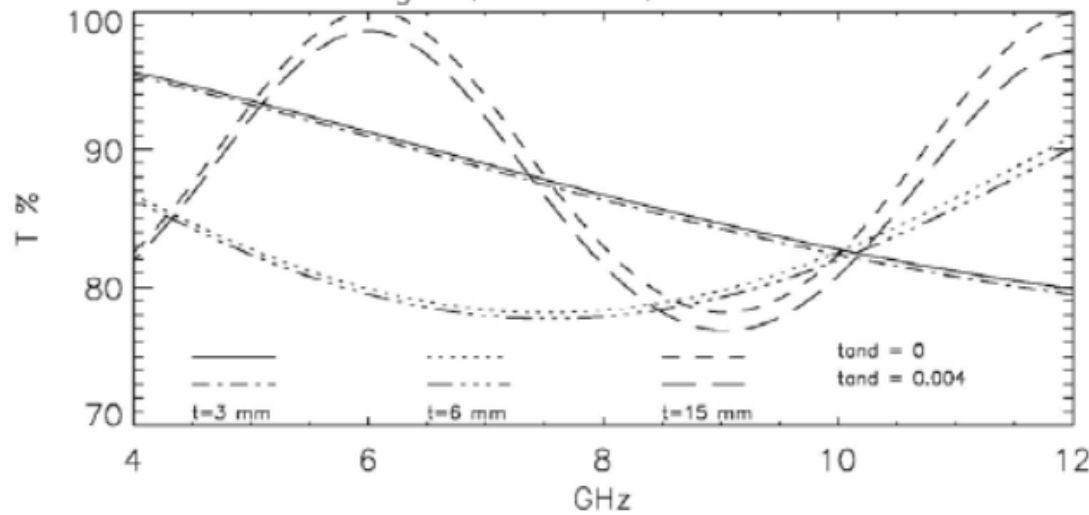




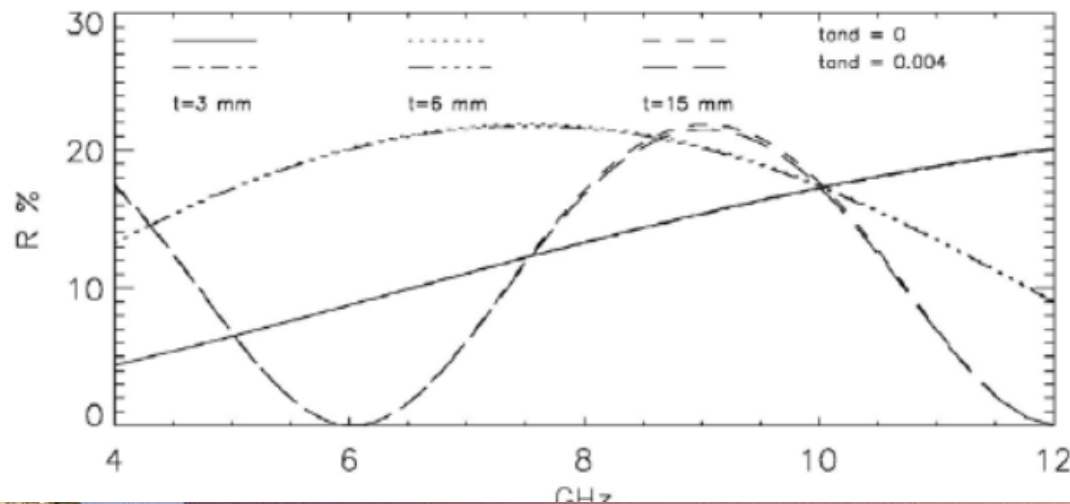


Material	e_r	$\tan \delta \times 10^{-4}$
Styrodur 3035CS (BASF) (Green IR filter)	1.04	0.3
Plexiglass (Vacuum window)	2.54	45.3
Styrofoam (Vacuum window protection)	1.03	1.5
Nylon 6 (Window ring lockout)	3.1-8.3	6-1900
Black Polyethylene (one layer 0.1mm)	2.7	10
Eccostock PP4 (Total of 5 layer of 1.7mm)	1.06	1
HDPE (about 0.06mm thickness covering the styrofoam)	2.3	1

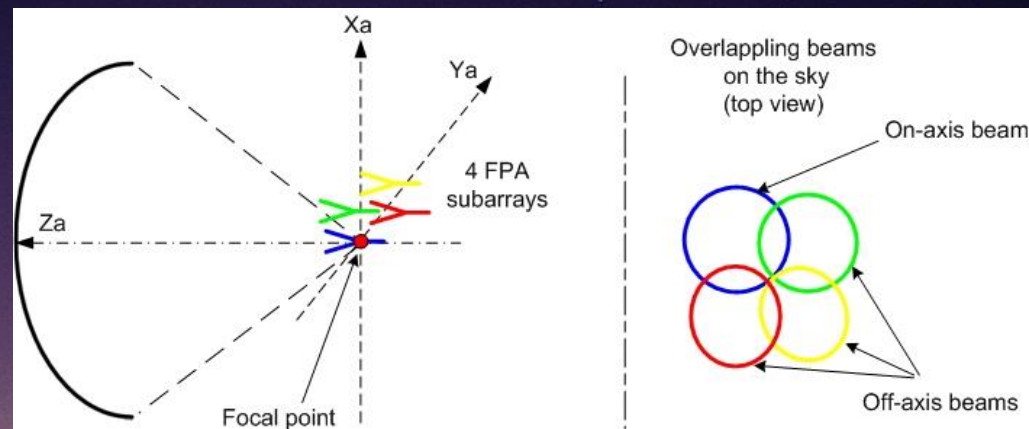
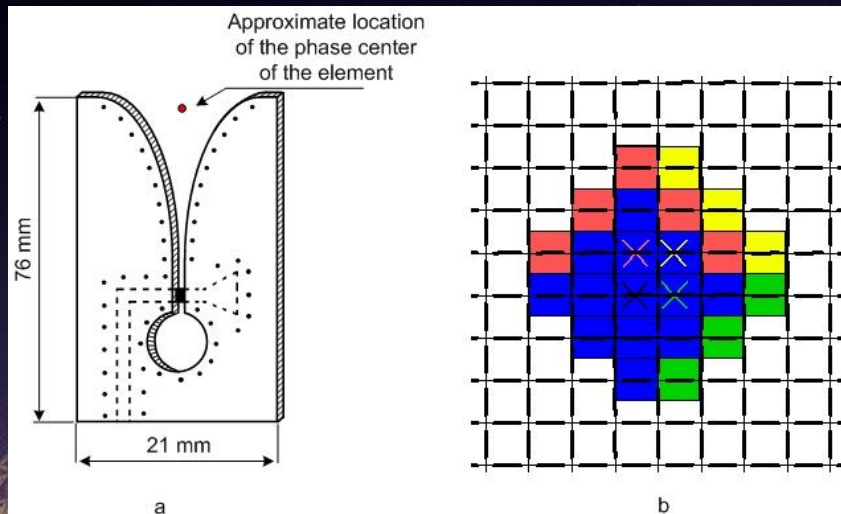
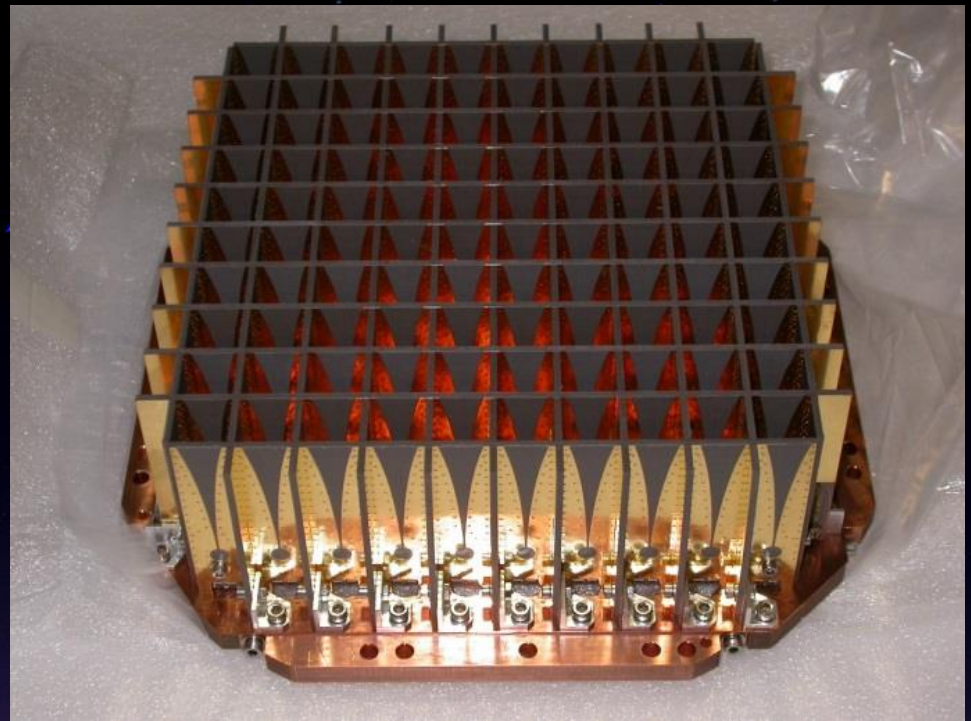
Plexiglas, $n=1.66$, $\tan\delta=0.004$



- ◆ Transmission and reflection losses
- ◆ High epsilon more significant than $\tan\delta$



Vivaldi array

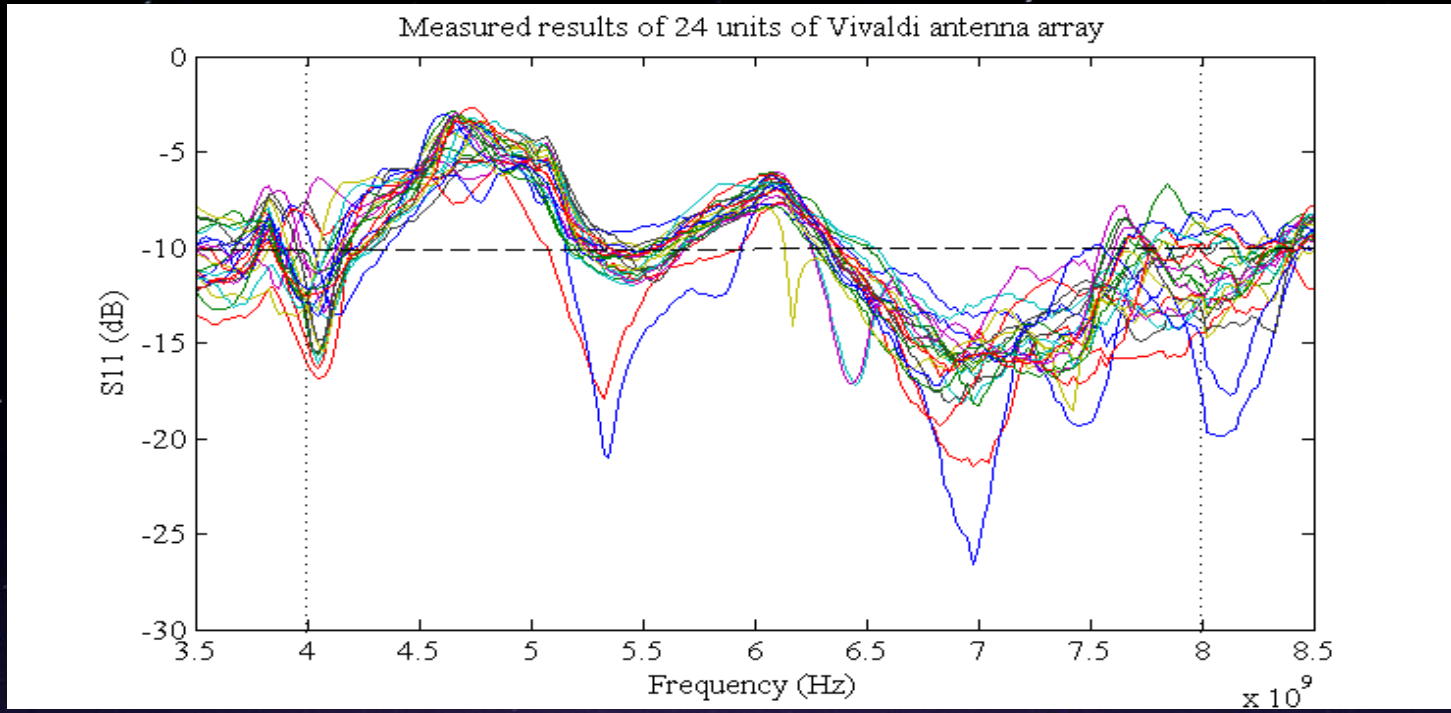


The geometry of the FPA element (a) and schematic of the FPA subarrays (b).

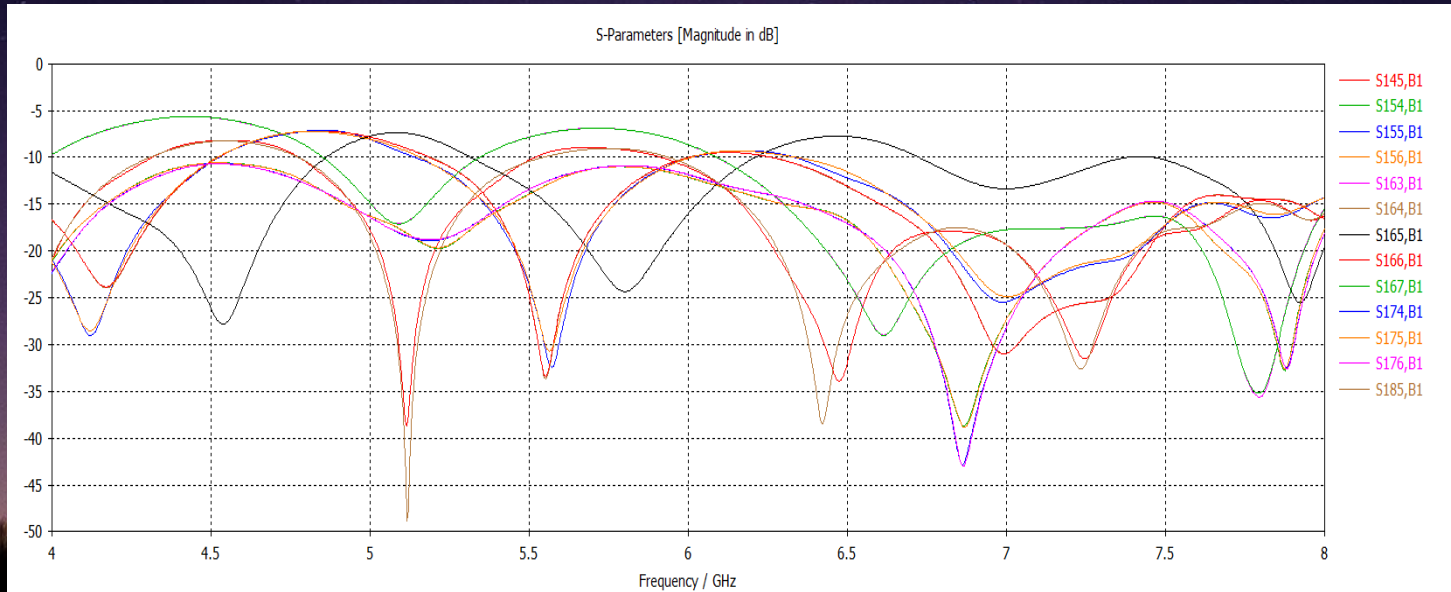
Positions of FPA subarrays in the focal region of reflector and corresponding beams on the sky

S parameter

Isolated ports
excite test by VNA



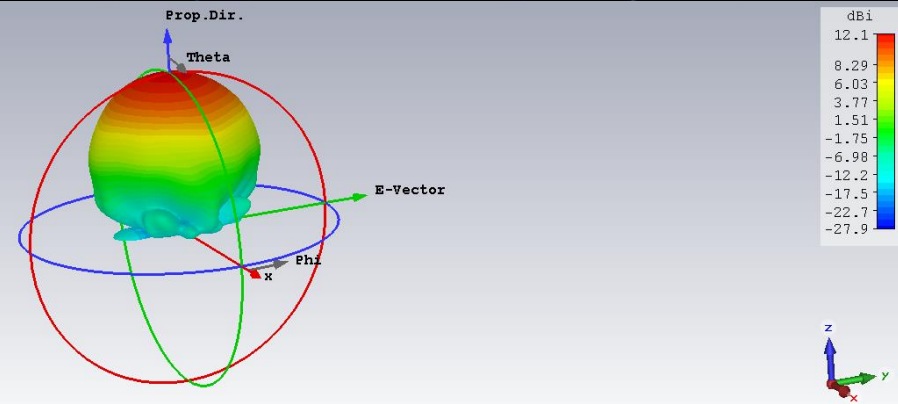
Active ports excite
simulation by CST



Farfield pattern 3D plot

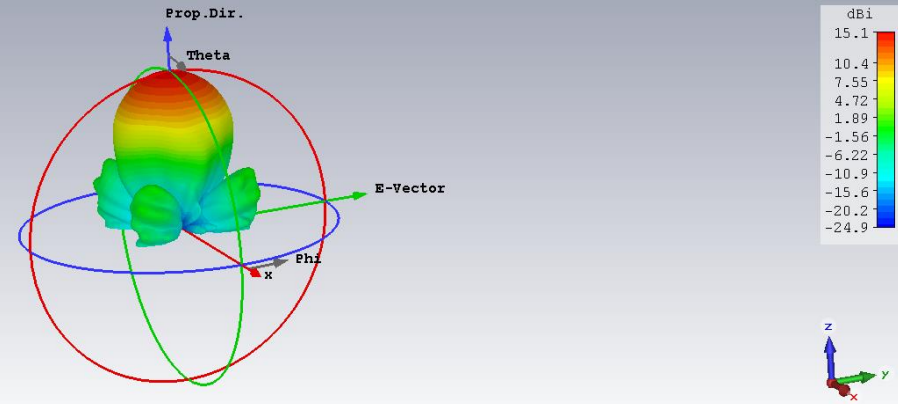
4G

Type	Farfield
Approximation	enabled ($kR \gg 1$)
Monitor	farfield (f=4) [B1]
Component	Abs
Output	Directivity
Frequency	4
Rad. effic.	-0.08122 dB
Tot. effic.	-0.9236 dB
Dir.	12.06 dBi



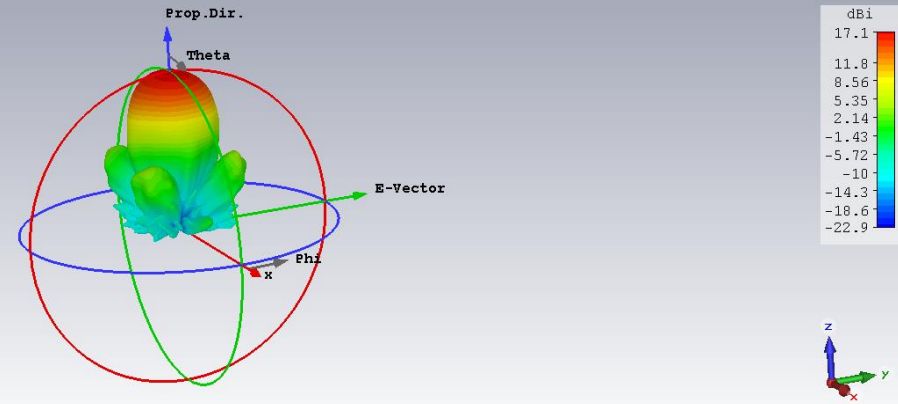
6G

Type	Farfield
Approximation	enabled ($kR \gg 1$)
Monitor	farfield (f=6) [B1]
Component	Abs
Output	Directivity
Frequency	6
Rad. effic.	-0.1053 dB
Tot. effic.	-0.8529 dB
Dir.	15.11 dBi

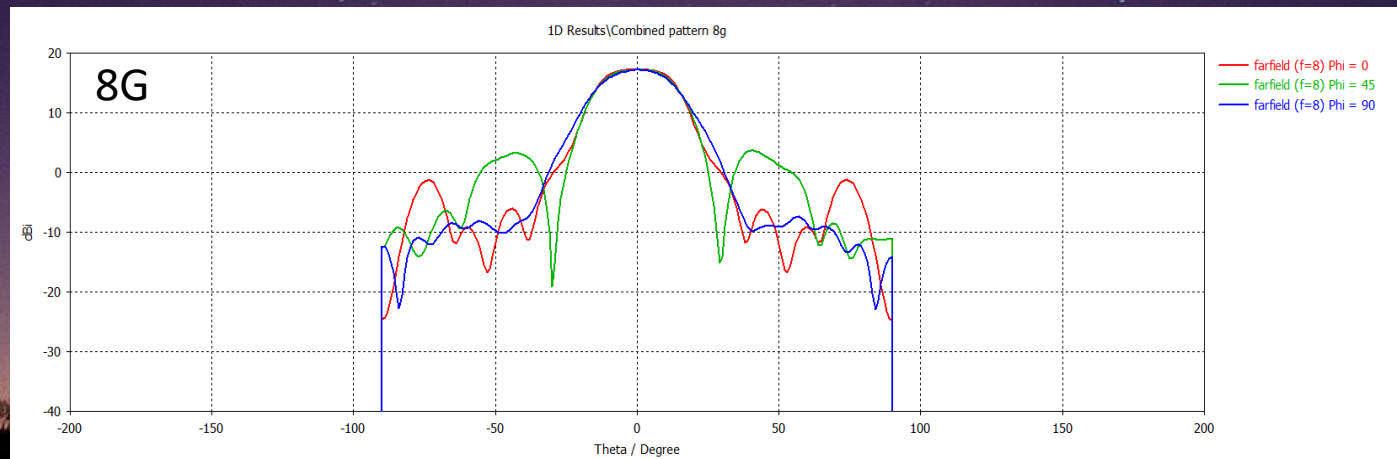
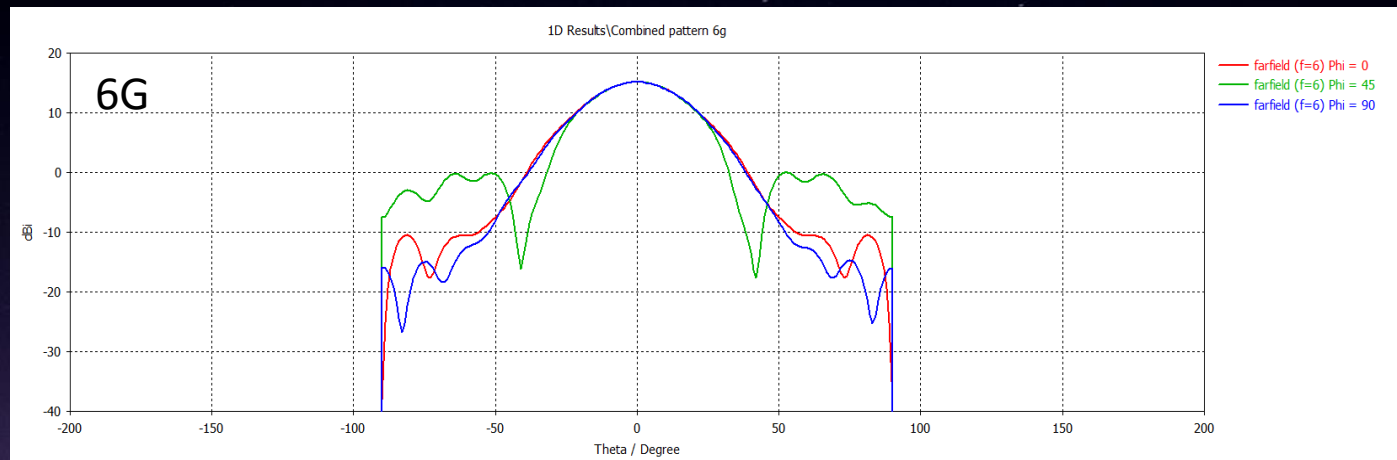
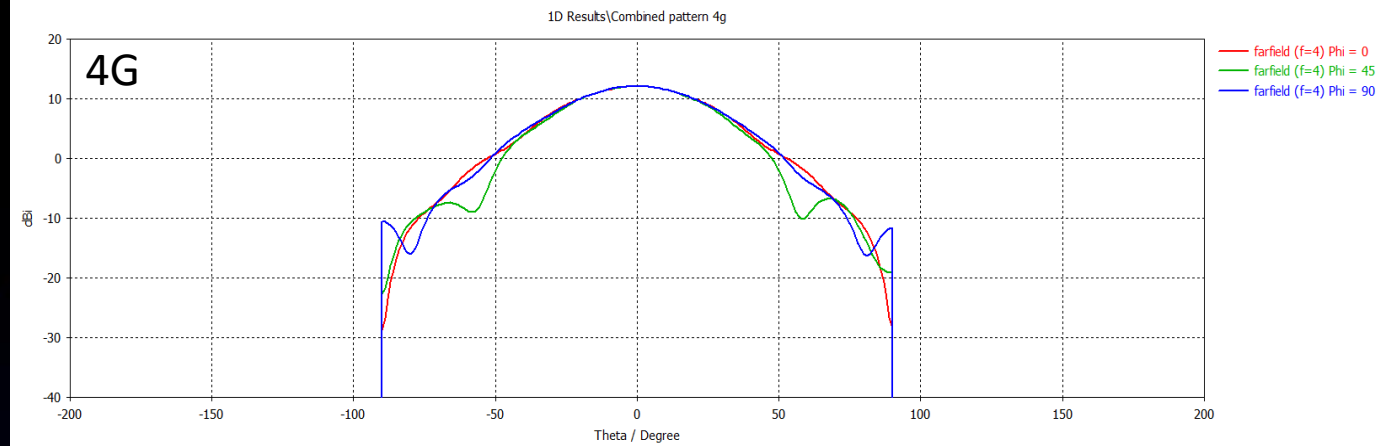


8G

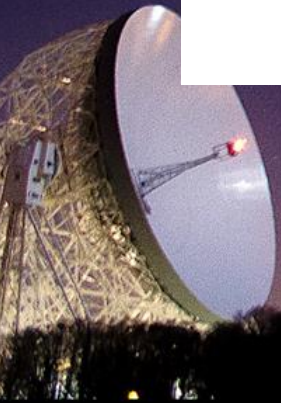
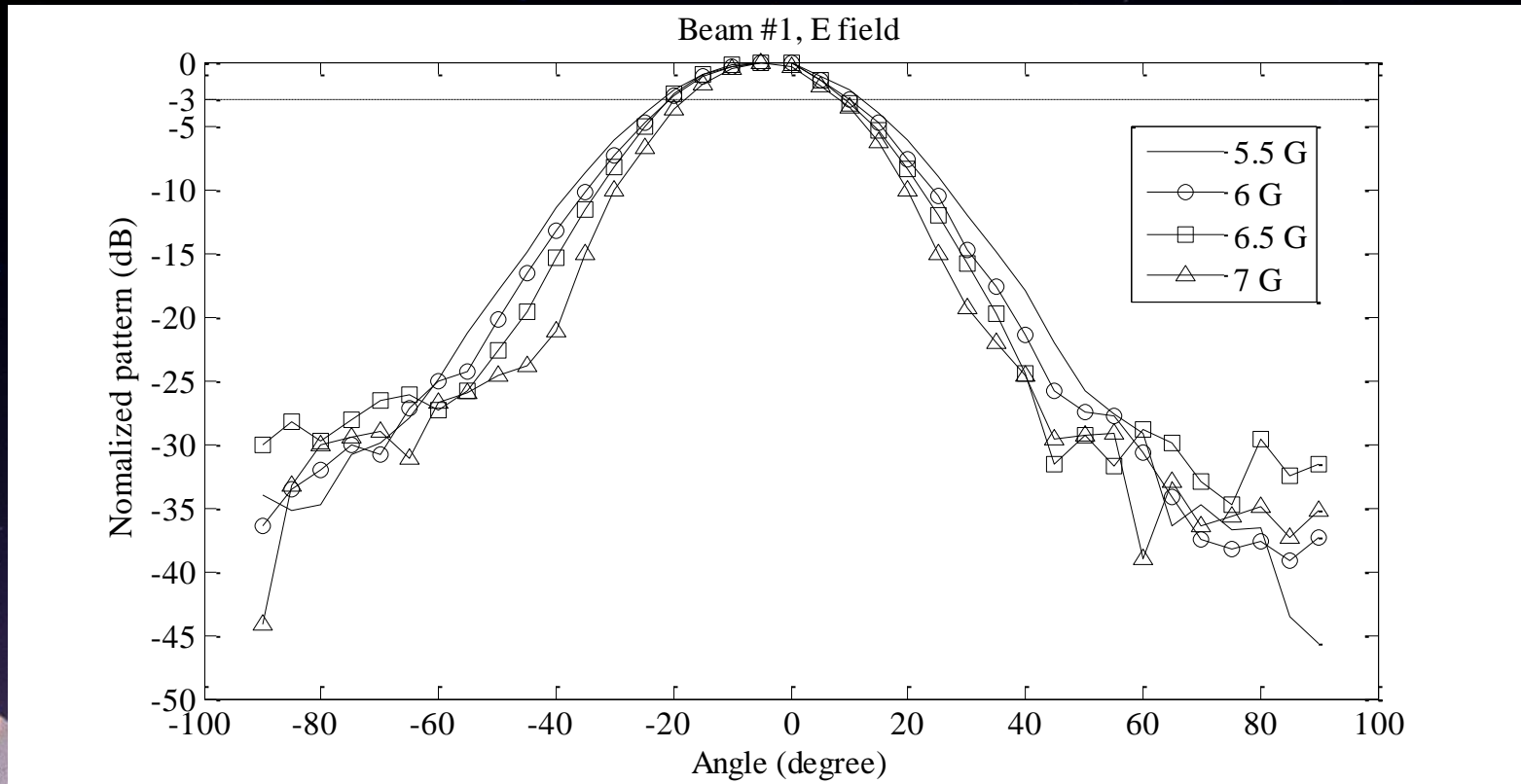
Type	Farfield
Approximation	enabled ($kR \gg 1$)
Monitor	farfield (f=8) [B1]
Component	Abs
Output	Directivity
Frequency	8
Rad. effic.	-0.1575 dB
Tot. effic.	-0.5198 dB
Dir.	17.13 dBi



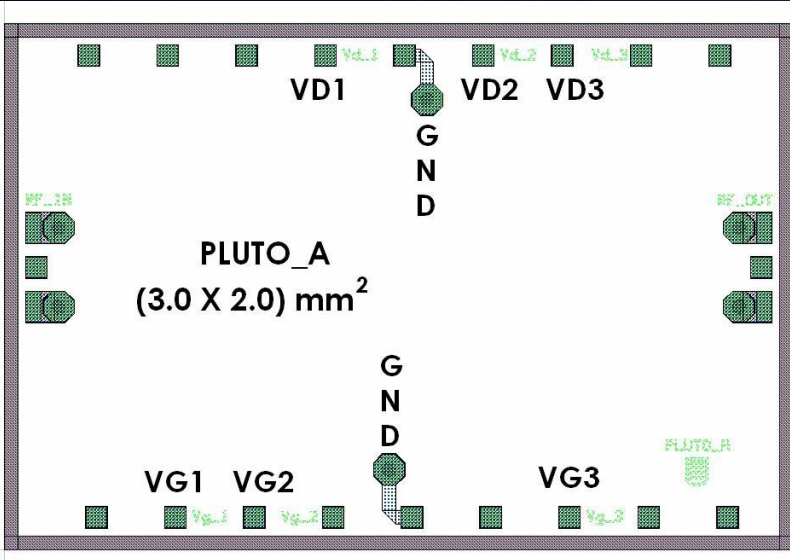
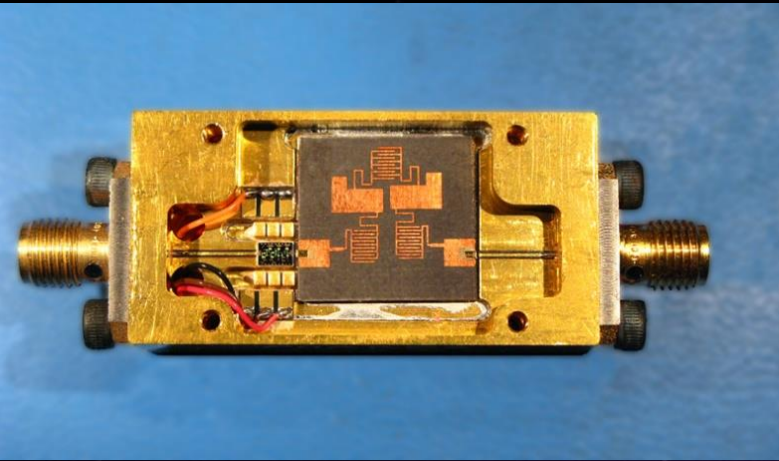
Farfield pattern 2D cut plot (Phi = 0, 45, 90 degree)



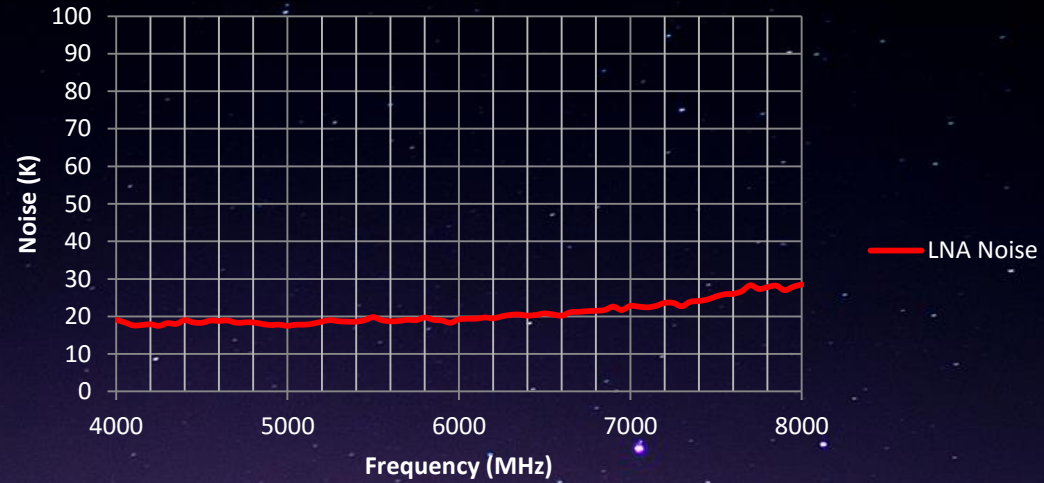
Farfield pattern test at anechoic chamber



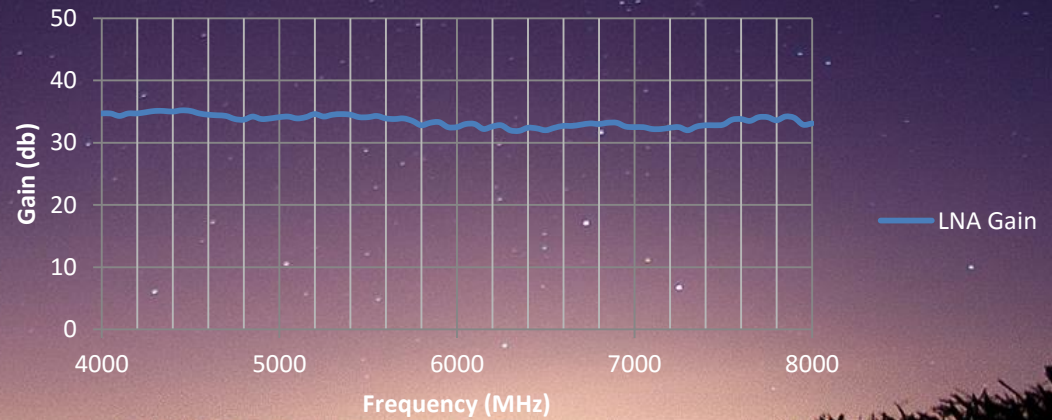
LNA



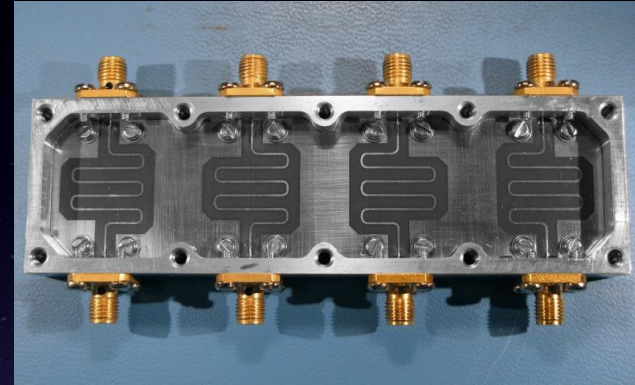
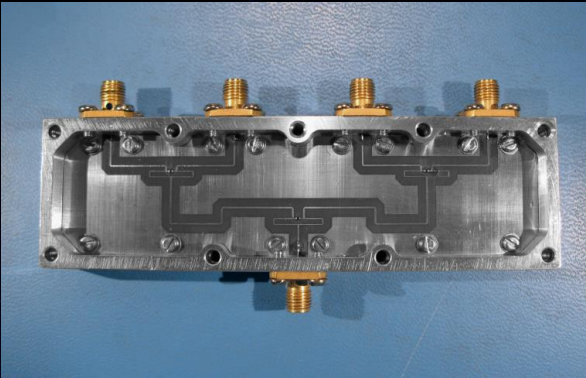
Pharos LNA10 Test1 EJB161115



Pharos LNA10 16K Test1 EJB161115



Splitter and Delay Line Module

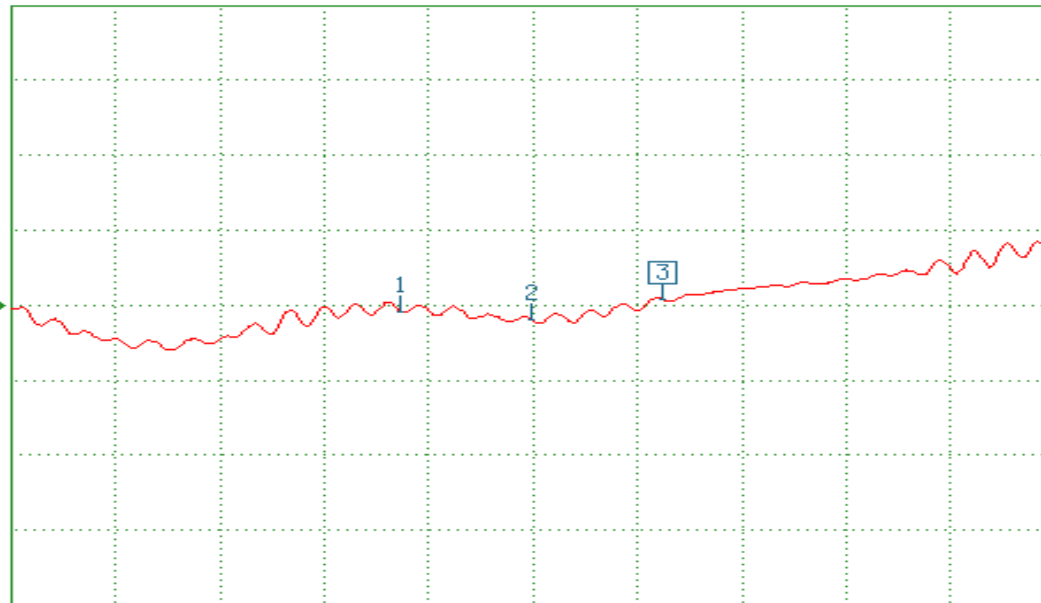


S21 FORWARD TRANSMISSION

PHASE

▶ REF = 0.00°

10.00°/DIV



4.000000000

GHz

8.000000000

CH 3 - S21
REFERENCE PLANE
0.0000 mm

▶ MARKER 3
6.500000000 GHz
0.79°

MARKER TO MAX
MARKER TO MIN

1 5.500000000 GHz
-0.94°

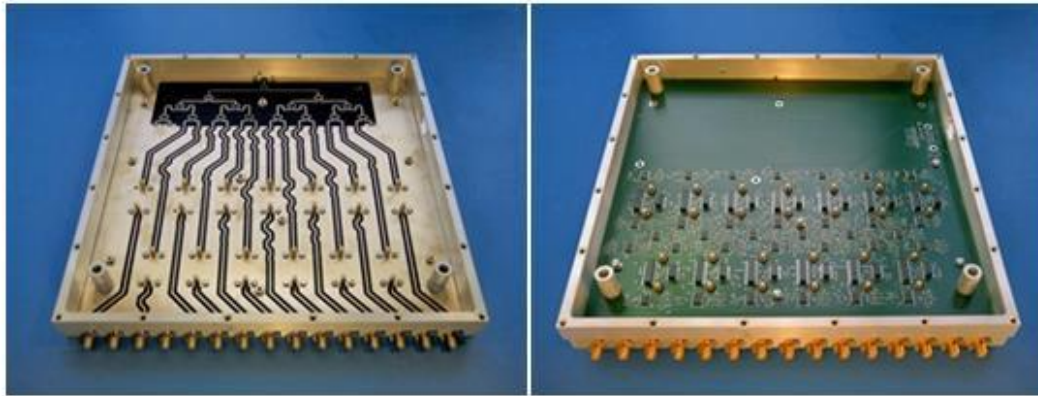
2 6.000000000 GHz
-2.03°

MARKER READOUT
FUNCTIONS



Beam former module

1. RF board
2. Digital control board
3. Phase and amplitude control module (PAC)



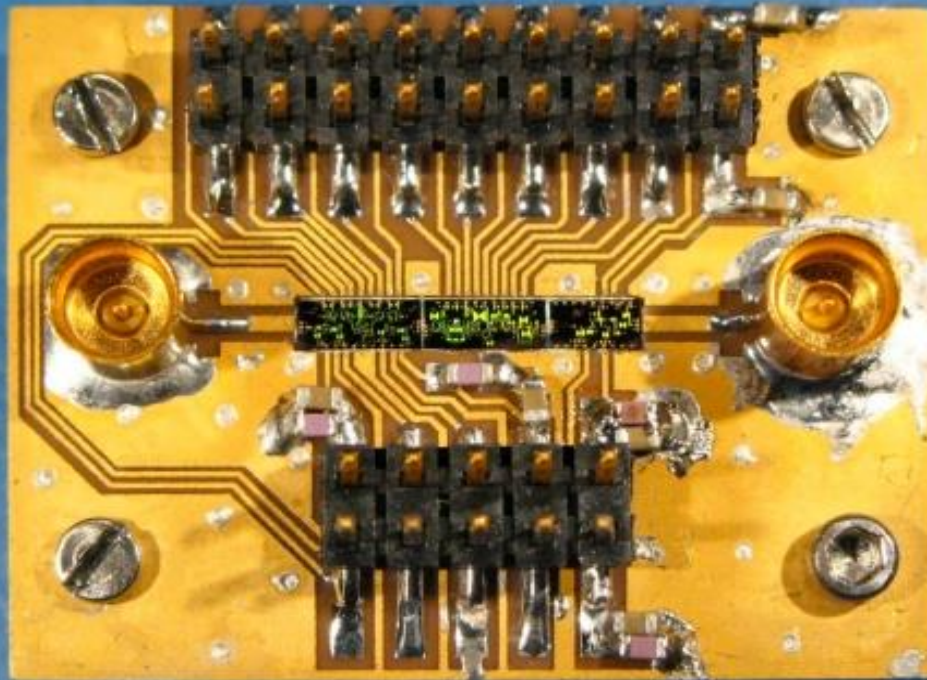
(a)



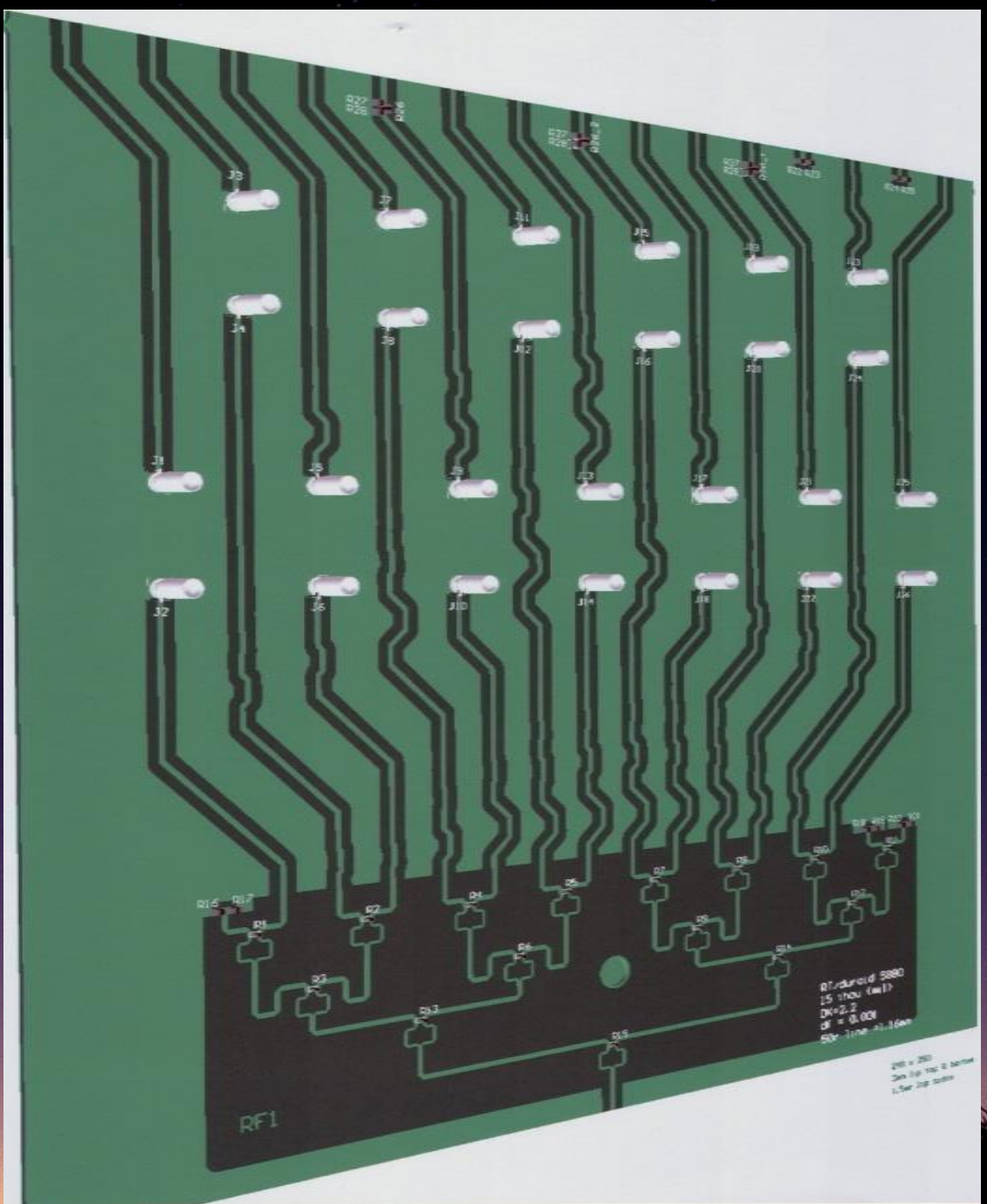
(b)



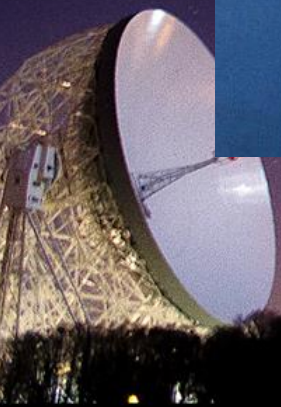
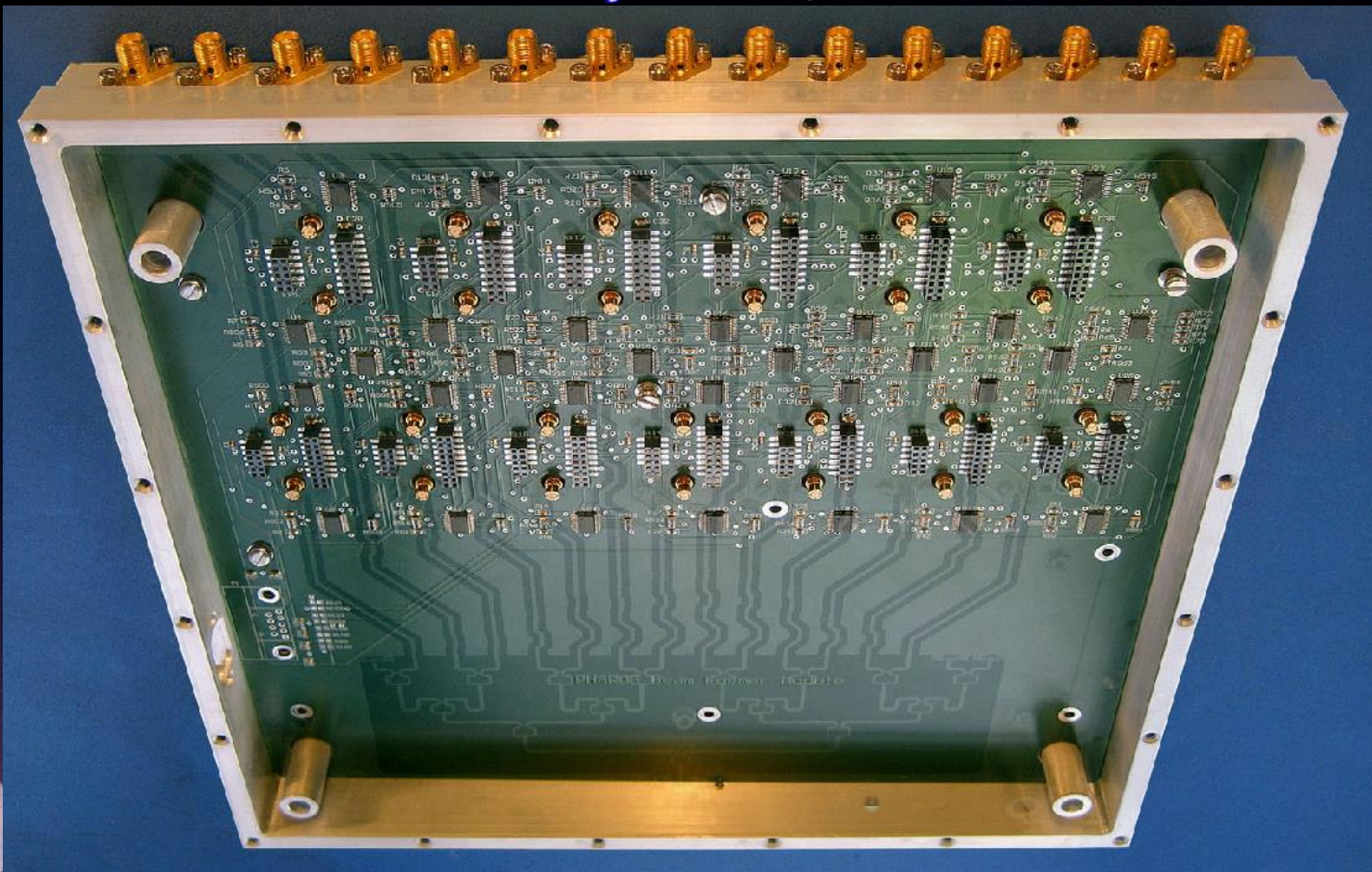
Phase and amplitude control module (PAC)



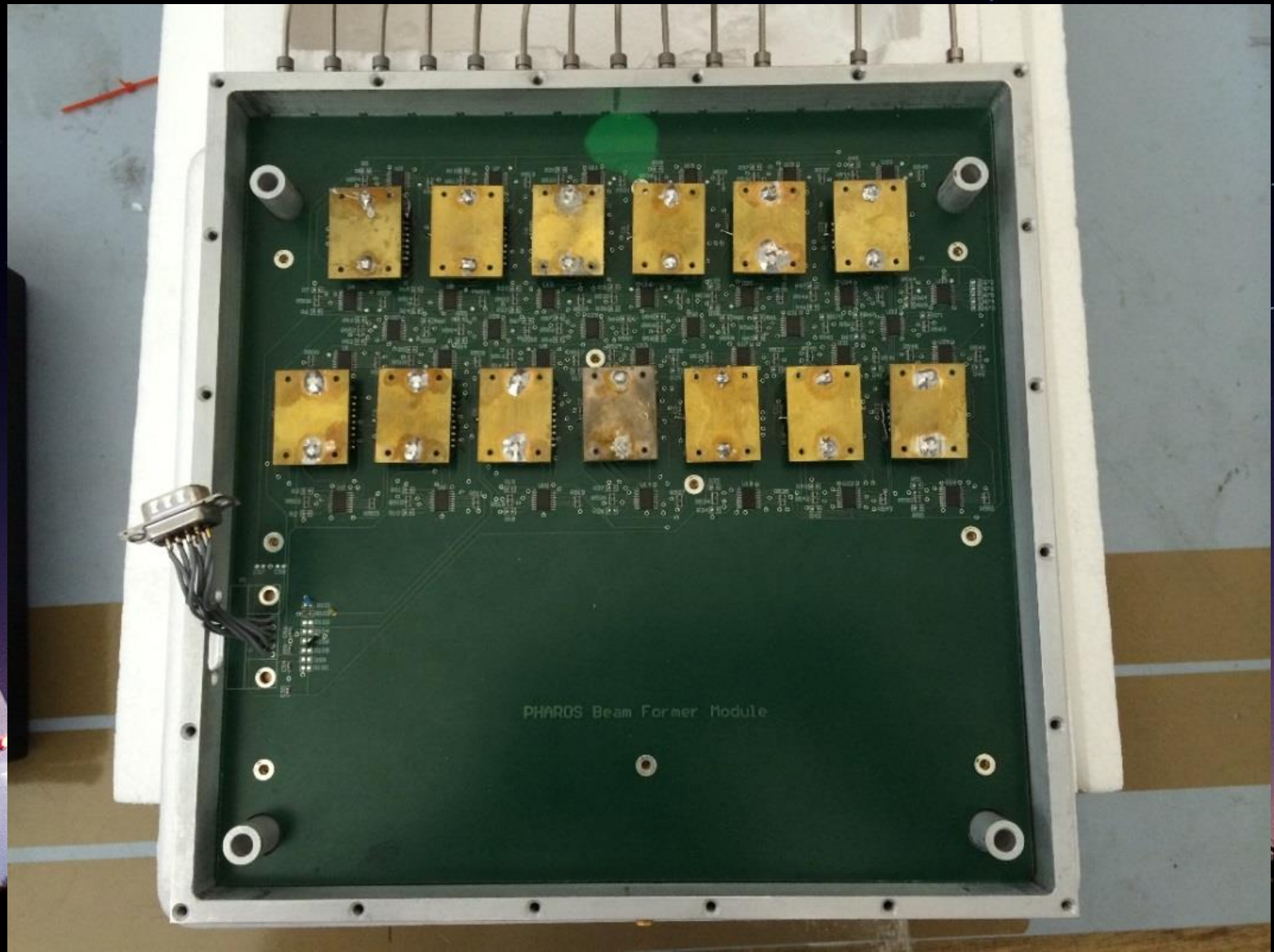
RF board



Digital control



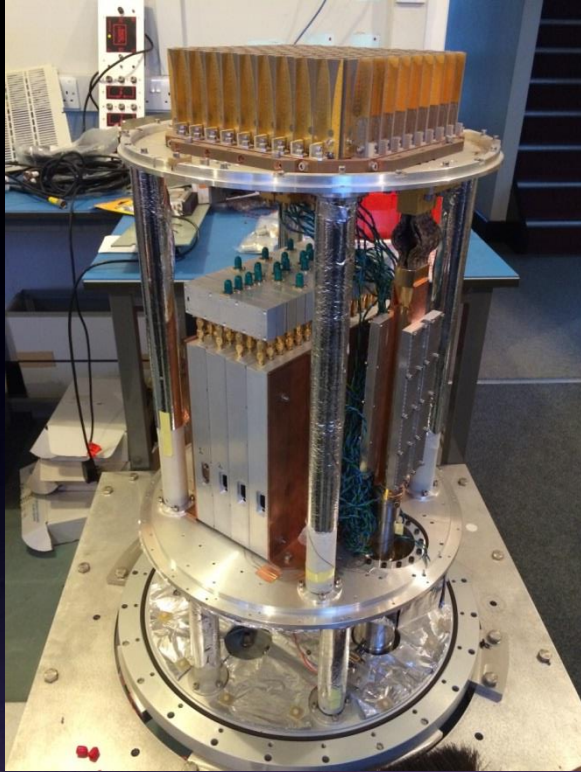
Integrated beam former board



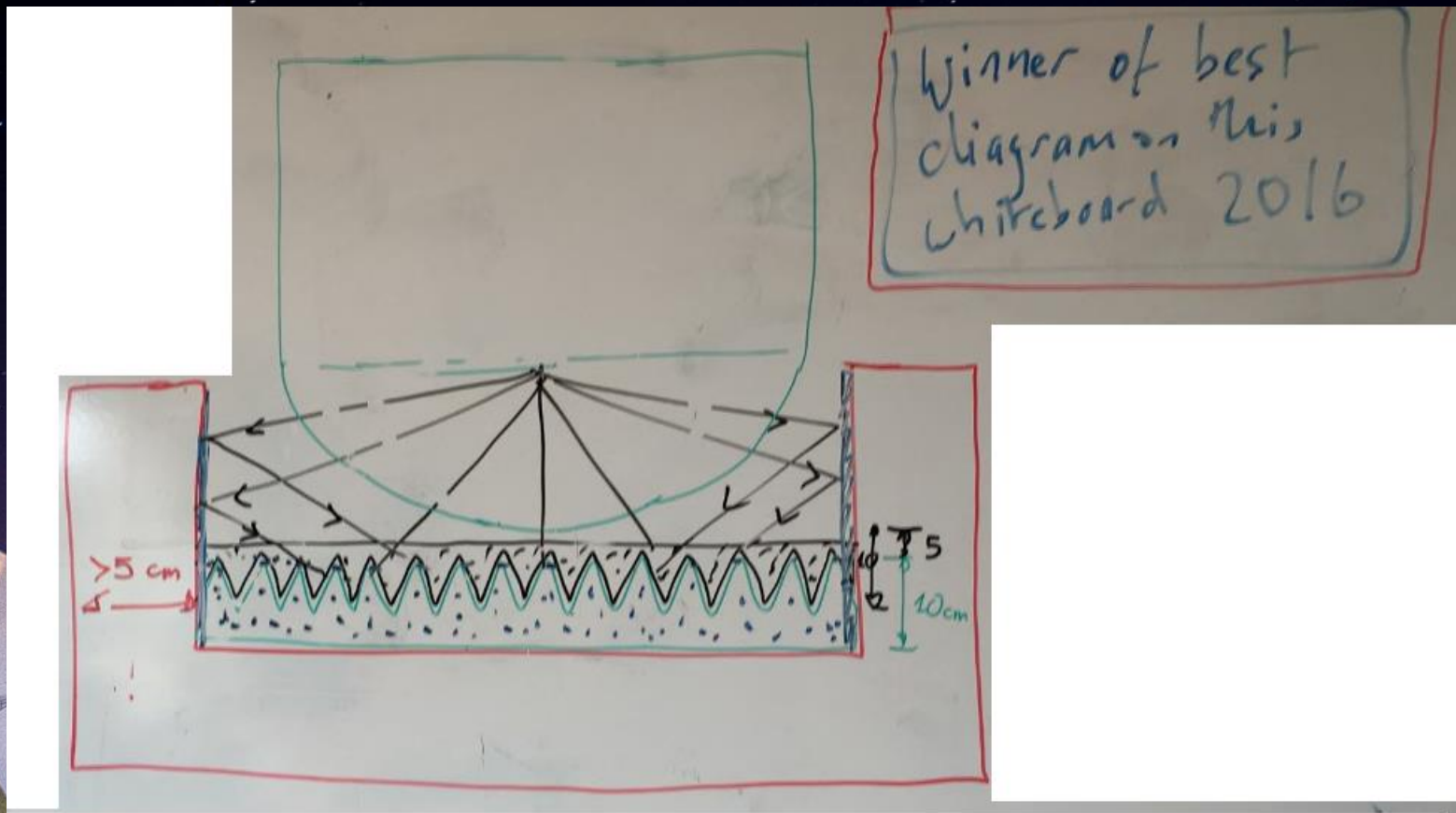
Beam former control UI

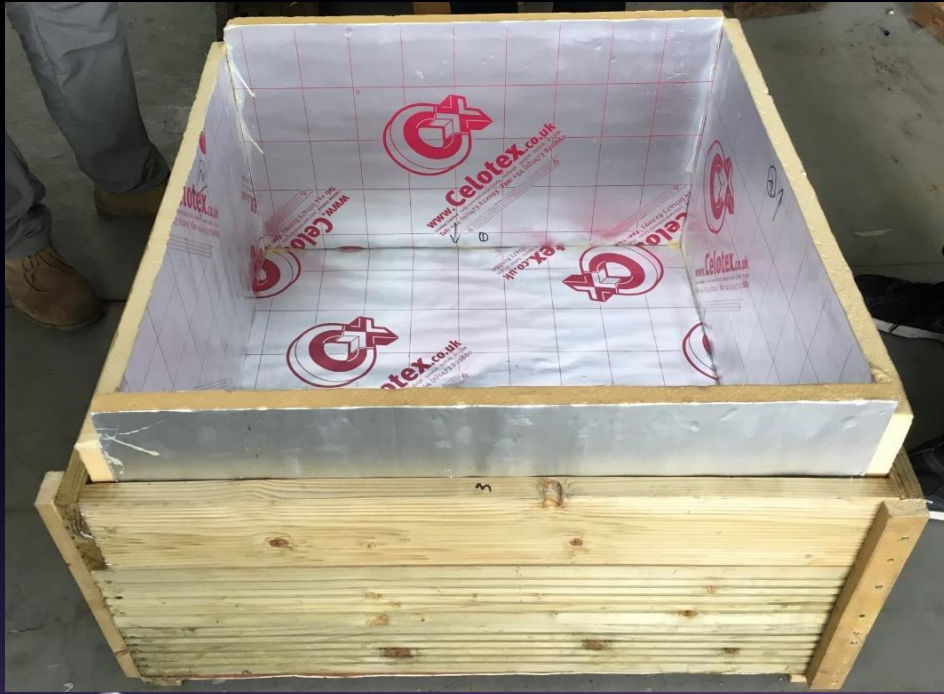
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
1												Port:	3		48			
2												Add:	G1S00	open	0			
3												No. in i2c	7	write	8			Initialise
4			0.0°								0.0°	No. in Add	12	read	6			Write
5			2-12								4-6	Hex	C		3			CommandButton6
6			0.0dB								0.0dB				48			Close
7		0.0°	0.0°	0.0°						0.0°	0.0°	0.0°			A			Read
8		2-13	2-5	2-11						4-7	4-2	4-13						Send All Data
9		0.0dB	0.0dB	0.0dB						0.0dB	0.0dB	0.0dB						Reset Controls
10	0.0°	0.0°	0.0°	0.0°	0.0°					0.0°	0.0°	0.0°	0.0°	0.0°				
11	2-6	2-2	2-1	2-4	2-10					4-8	4-3	4-1	4-5	4-12				
12	0.0dB	0.0dB	0.0dB	0.0dB	0.0dB					0.0dB	0.0dB	0.0dB	0.0dB	0.0dB				
13		0.0°	0.0°	0.0°							0.0°	0.0°	0.0°	0.0°				
14		2-7	2-3	2-9							4-9	4-4	4-11					
15		0.0dB	0.0dB	0.0dB							0.0dB	0.0dB	0.0dB					
16			0.0°								0.0°							
17			2-8								4-10							
18			0.0dB								0.0dB							
19																		
20					<input checked="" type="checkbox"/> Enable													
21																		
22																		
23																		
24																		
25																		
26			0.0°								0.0°							
27			1-10								3-8							
28			0.0dB								0.0dB							
29		0.0°	0.0°	0.0°						0.0°	0.0°	0.0°						
30		1-11	1-4	1-9						3-9	3-3	3-7						
31		0.0dB	0.0dB	0.0dB						0.0dB	0.0dB	0.0dB						

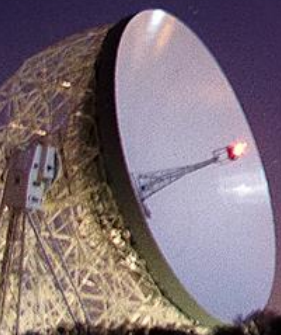
Integration



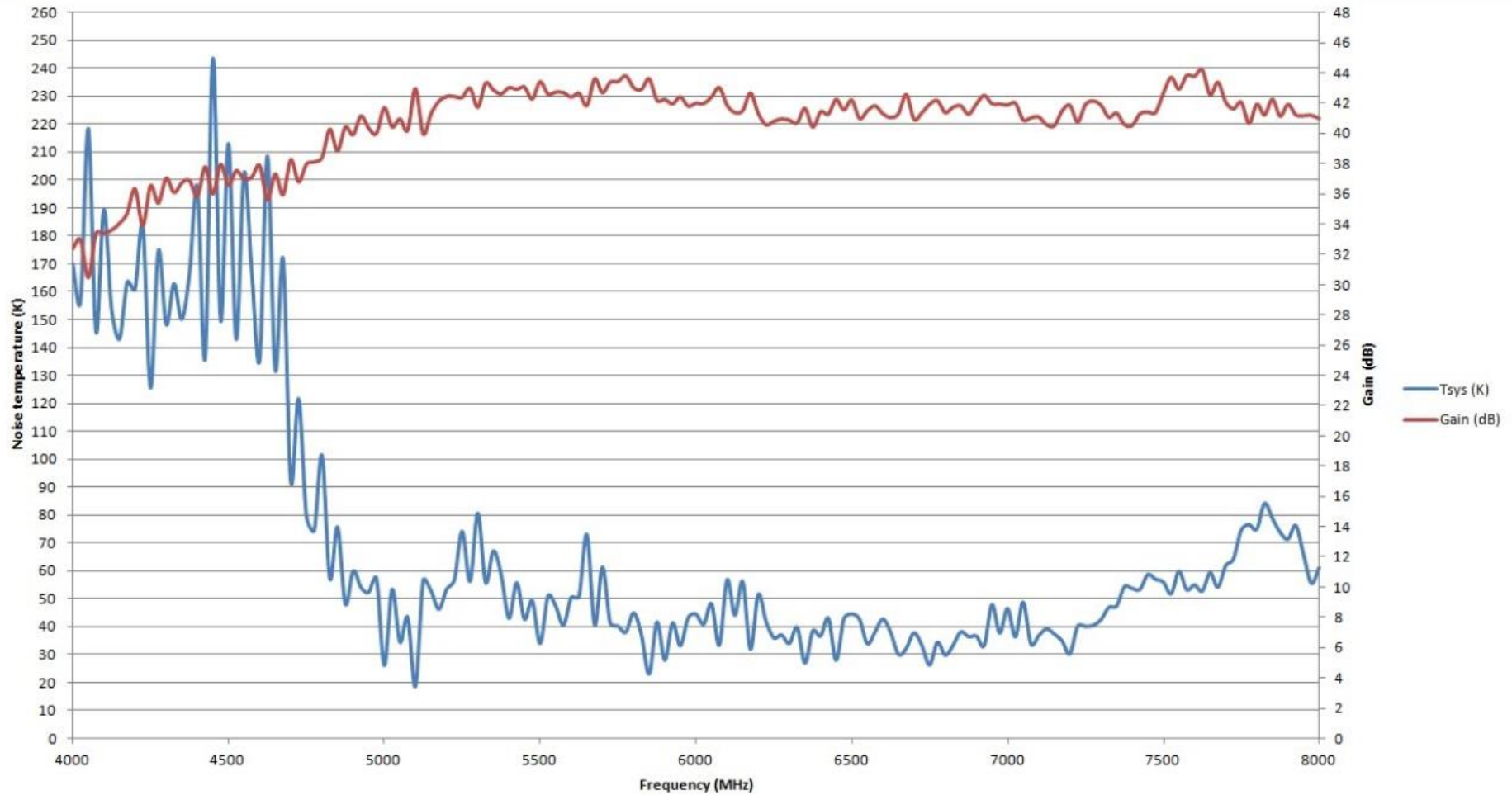
Noise temperature test set up plan a:







Noise temperature and gain



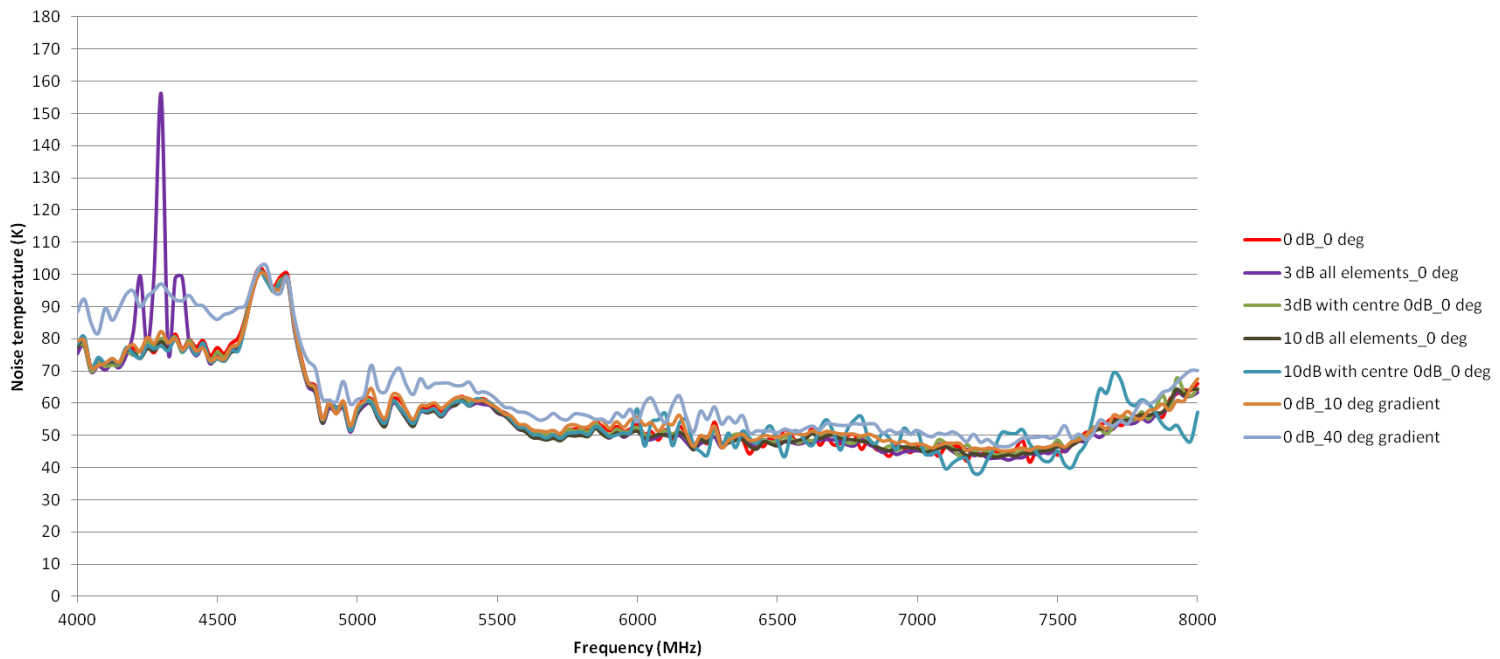
Test set up plan B:



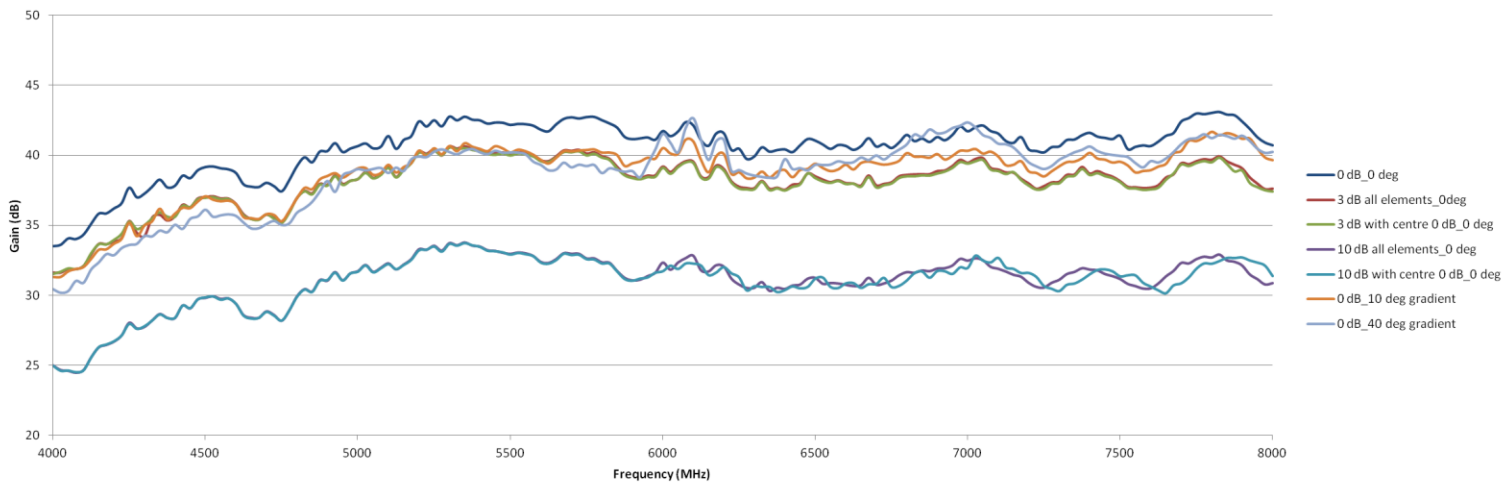
Clear SKY !



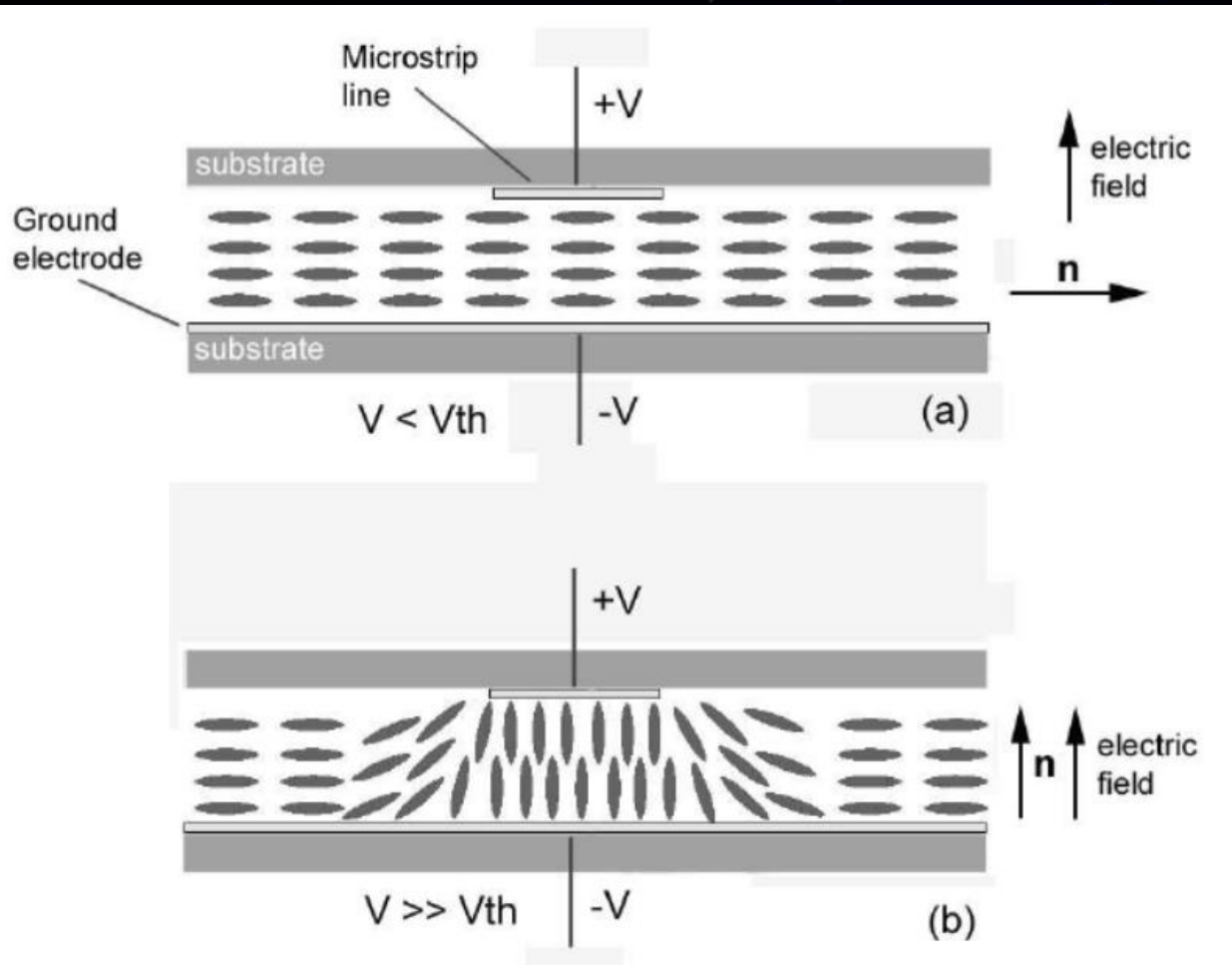
Results



PHAROS Tsys test at JBO

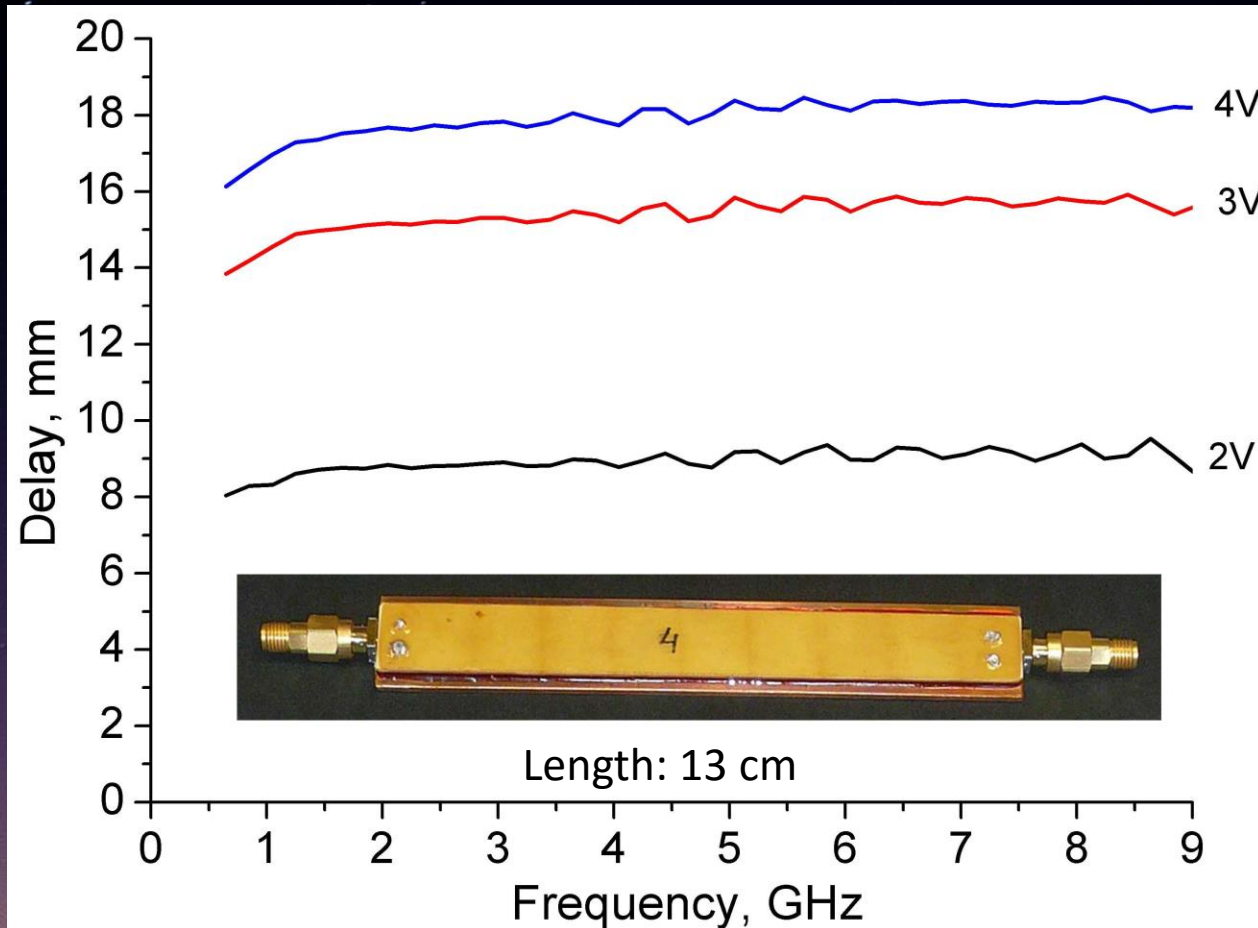


Liquid Crystal Delay line

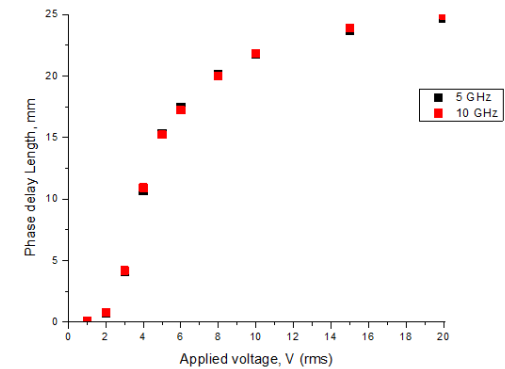
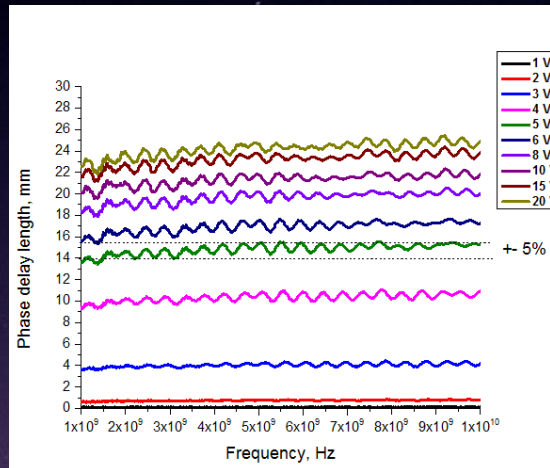
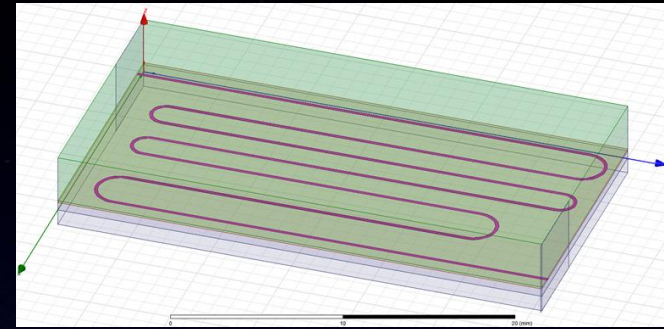


Cross section of an LC filled electrically tunable microstrip line.

Liquid Crystal Delay line – 1st generation

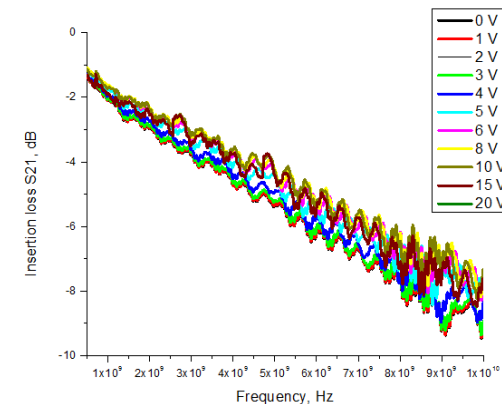


Liquid Crystal Delay line – 2nd generation

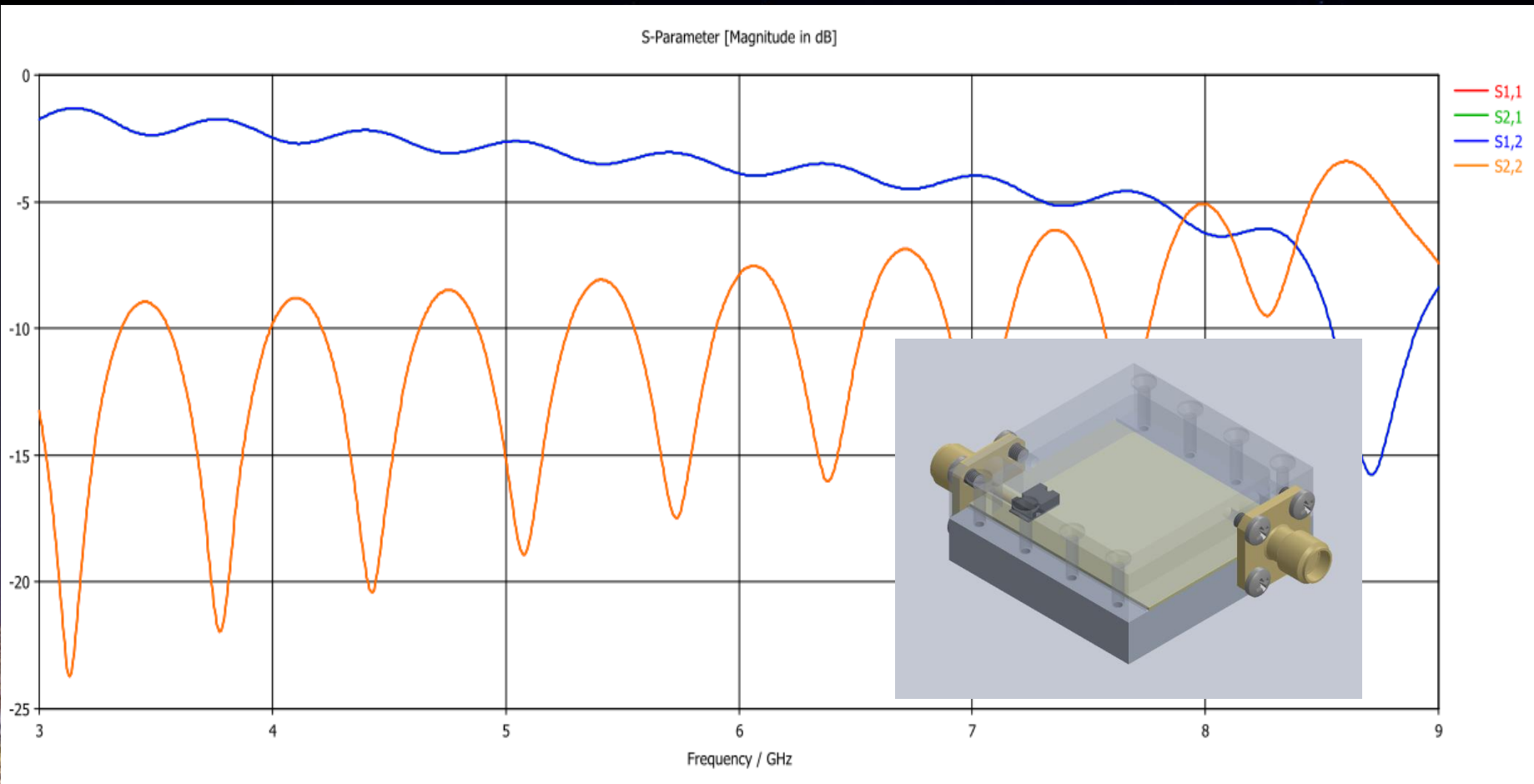


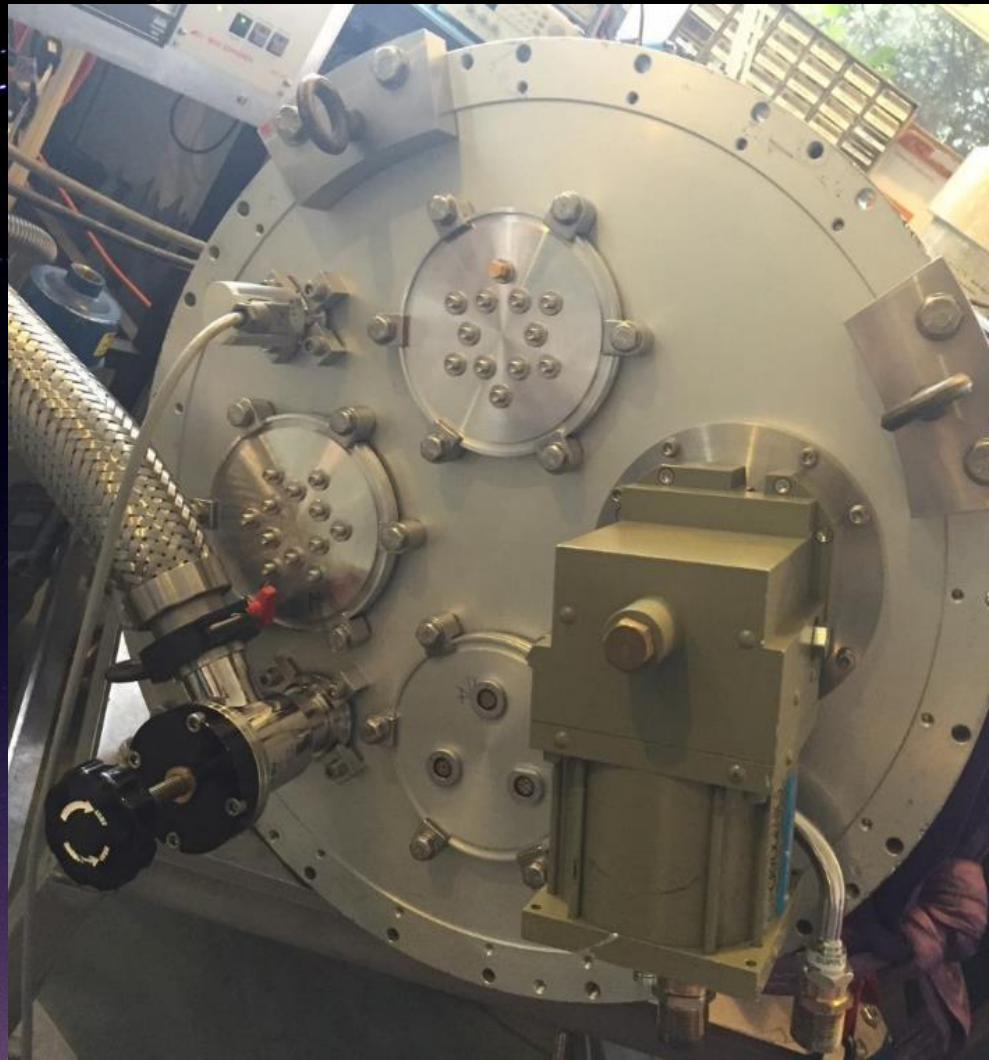
Device performance (0.5 - 10 GHz):

- Delay length \sim 24 mm (20 V rms)
- Insertion loss $<$ -10 dB at freq. $<$ 10 GHz
- Delay length variation $<$ \pm 5%



Liquid Crystal Delay line – 3rd generation





Future plan

- More tests on going,
- Mount on Lovell and test,
- New LNAs to reduce noise temperature,
- New structure of liquid crystal lines,
- Extend to more beams.



Thanks !

Groups:

JBO, Manchester.

Cavendish lab, Cambridge.

CAPE, Cambridge.

